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The Kingdom of Norway

N001/113

PCT/NO 01 / 00113

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| REC'D | 17 APR 2001 |
| WIPO  | PCT         |

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# Bekreftelse på patentsøknad nr

*Certification of patent application no*

# 2000 1360

Det bekreftes herved at vedheftede dokument er nøyaktig utskrift/kopi av ovennevnte søknad, som opprinnelig inngitt 2000.03.15

*It is hereby certified that the annexed document is a true copy of the above-mentioned application, as originally filed on 2000.03.15*

## PRIORITY DOCUMENT

SUBMITTED OR TRANSMITTED IN  
COMPLIANCE WITH RULE 17.1(a) OR (b)

2001.03.27

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Seksjonsleder

*Ellen B. Olsen*

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**PATENTSTYRET**  
Styret for det industrielle rettsvern

15. MAR 00 201360

Behandler medlem: EH  
Int. Cl. H 01 L

Utfylles av styret

# Søknad om patent.

Søknadsskriv

2000-03-15

la - c

Søkers/fullmektigens referanse  
lengre hvis ønsket:

Opti 51prNO

Oppfinnelsens  
benøvnelse:

Hvis søknaden er  
en internasjonal søknad  
som videreføres etter  
patentlovens § 31:

Søker:

Namn, bopel og adresse.  
(Hvis patent søkes av flere:  
opplysning om hvem som skal  
være beremyndighet til å motta  
meddelelser fra Styret på vegne  
av søkerne).

(Fortsett om nødvendig på neste side)

Oppfinner:

Namn og (privat) adresse

(Fortsett om nødvendig på neste side)

Fullmektig:

Hvis søknad tidligere  
er inngitt i eller  
utenfor riket:

(Fortsett om nødvendig på neste side)

Hvis avdelt søknad:

Hvis utskilt søknad:

Deponert kultur av  
mikroorganisme:

Utlevering av prøve av  
kulturen:

Vertikale elektriske forbindelser i stabel

Den internasjonale søknads nummer

Den internasjonale søknads inngivelsesdag

THIN FILM ELECTRONICS ASA

Postboks 1872 Vika

N-0124 OSLO

oppgis senere

Prioritet kreves fra dato ingen sted nr.

Prioritet kreves fra dato sted nr.

Prioritet kreves fra dato sted nr.

Den opprinnelige søknads nr.: og deres inngivelsesdag

Den opprinnelige søknads nr.: begjært inngivelsesdag

☐ Søknaden omfatter kultur av mikroorganisme

☐ Prøve av den deponerte kultur av mikroorganisme skal bare utleveres til en særlig sakkyndig,

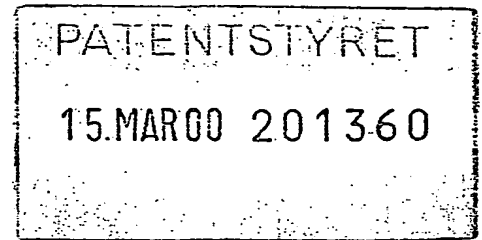
jfr. patentlovens § 22 åttende ledd og patentforskriftens § 38 første ledd

Fig. nr. ....

2000 1360

Angivelse av tegnings-  
figur som ønskes  
publisert sammen med  
sammendraget

Pr000314.invrecordIR00-2.doc



**INVENTION RECORD**

**\*01\_SER:** [Serial number, e.g. IR98-2]  
**IR00-2**

**02\_DAT:** [Date of record, day-month-year]  
**Jan. 17, 2000**

**03\_DEN:** [Title/Denomination of the invention]  
**Vertical interconnects in stack**

**04\_ORI:** [Origin; company or institution names]  
**Thin Film Electronics ASA**

**05\_PRO:** [Project name and identification]  
.....

**06\_CON:** [Contact person at origin]  
**Per-Erik Nordal**

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**09\_INV:** [Lists inventors (tentative); affiliation if not at origin, private addresses]  
**Per-Erik Nordal , Hans Gude Gudesen,+++++++ .....**

**10\_TFI:** [Technical field of the invention]  
**Non-volatile memories based on ferroelectrics and/or electrets**

**11\_PRA:** [Prior art, e.g. books, papers, reports, patents etc., incl. those issued at origin]  
**None**

**12\_OBJ:** [Lists objects, purposes or advantages linked with the invention]  
**Object and purpose: Create electrical interconnects between layers and/or between layers and an underlying substrate, in a memory and/or processing device that incorporates a stack of two or more sheet- or film-like functional parts that partially or completely overlap each other.**

**13\_SUM:** [Short description of subject matter]  
**Objects, purposes and advantages of invention are achieved by sequentially adding one layer at a time to the stack, with electrical connections to/from each layer being led out to the edge of the layer in question and down the step at the edge to the top of the underlying layer or the substrate and creating electrical contact with circuitry already established at this lower level. With thin sheets in the stack, low step heights result, and conducting lines can be created by**



manufacturing-friendly techniques, capable of negotiating the step without problems. Tapering of the edges, etc, may be used to promote the edge connection process. By repeating this process layer by layer, connections can be created through a stack that includes a large number (hundreds or thousands) of layers, without resorting to penetrating vias that require etching, drilling or punching through the layers themselves. Fig.1 shows examples of simple stacking arrangements: In Fig.1a, the stack contains square sheets arranged on top of each other in a symmetric pyramid structure. In Fig.1b, more sheet area in the stack is gained by a staircase structure, as shown. The choice between different alternatives as exemplified in Figs. 1a and 1b is dependent on e.g. the number of lines to be led to/from each layer, cost and complexity in manufacturing, overall electronic design architecture, etc.

14\_CHR: [Lists specific novel features characterizing and supporting the invention]

The advantages of the present invention are particularly evident when the number of layers in the stack becomes large. According to the invention, each connectivity step involves only one layer thickness, in contrast to a via solution capable of linking all layers in the stack.

\*15\_PSE: [Patentability search identification]

\*16\_TFR: [Tentative term for filing a patent application]

17\_APP: [Lists additional material, including drawing figures, sent under separate enclosure]

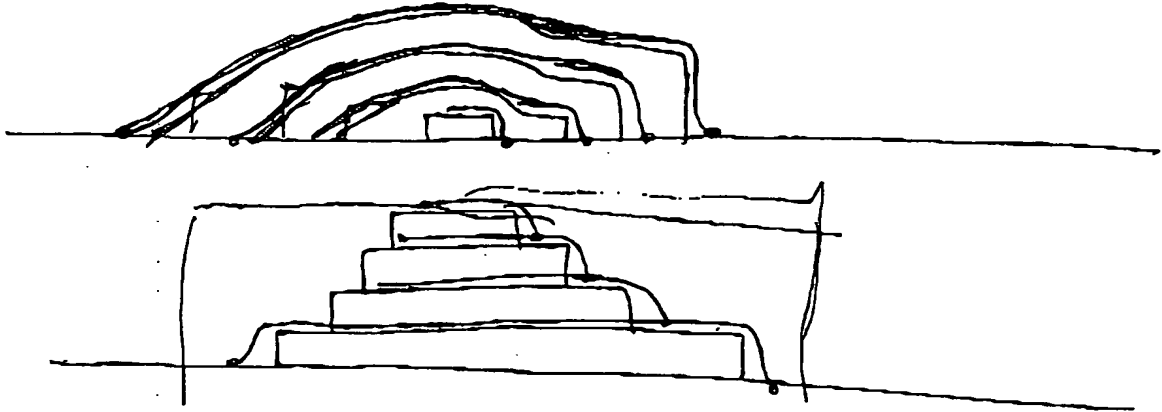
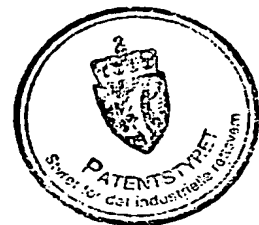
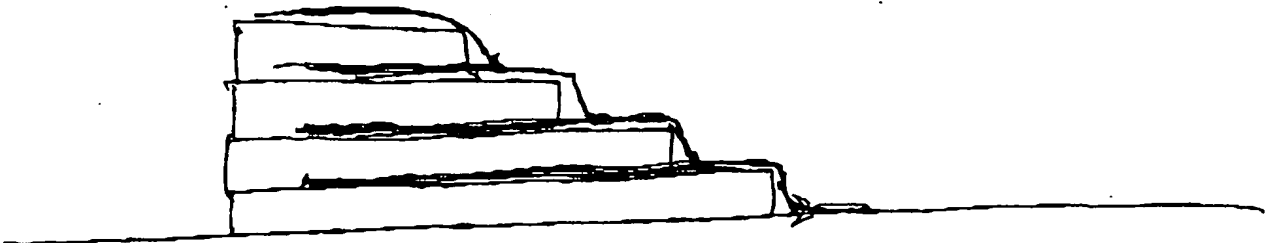
18\_RES: [Resource persons, e.g. advisers or consultants without claim to inventorship]

\*19\_RCV: [Received by IPR & I.D, day-month-year]

\*20\_NOT: [Notarization date & authority for obtaining a legal date of conception]



1R00-2

Fig 1aFig 1b

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